ABSTRACT

[0028] Disclosed is a virtual dual-port synchronous RAM device, system, and method, wherein the design requires minimal hardware cost compared with a dual-port RAM architecture or the traditional architecture used with a single-port RAM. Disclosed is a read/write memory device including means to accept signals from a first host and a second host, the first host having a first clock and the second host having a second clock, the signals including a first clock signal and a second clock, a clock switching means for switching between the first clock signal and the second clock signal, a single-port random access memory (RAM) module for storing data, and a RAM clock for synchronizing the clock signals with the RAM module.